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INTERNATIONAL APPLICATION NO. **PCT/SG98/00031**	INTERNATIONAL FILING DATE **30 April 1998 (30.04.1998)**	PRIORITY DATE CLAIMED **30 April 1998 (30.04.1998)**

TITLE OF INVENTION
AUTOMATIC BRIGHTNESS LIMITATION FOR AVOIDING VIDEO SIGNAL CLIPPING

APPLICANT(S) FOR DO/EO/US
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Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☒ is transmitted herewith (required only if not transmitted by the International bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   a. ☒ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 16 below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☐ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information:
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Samuel Hall

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U.S. APPLICATION NO. (If known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
Unknown 09/674355	**PCT/SG98/00031**	**851663:417USPC**

17. ☒ The following fees are submitted:

Basic National Fee (37 CFR 1.492(a)(1)-(5)):

Search Report has been prepared by the EPO or JPO ..... $ 860.00

International preliminary examination fee paid to USPTO (37 CFR 1.482) ..... $ 690.00

No international preliminary examination fee paid to USPTO (cu CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) ..... $ 710.00

Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO $1000.00

International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) ..... $ 100.00

CALCULATIONS PTO USE ONLY

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Claims	Number Filed	Number Extra	Rate		
Total Claims	17 - 20 =	0	x $ 18.00	$0.00	
Independent Claims	4 - 3 =	1	x $ 80.00	$80.00	
Multiple dependent claim(s) (if applicable)			+ $270.00	$270.00	
TOTAL OF ABOVE CALCULATIONS =				$1340.00	
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Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property) +				$.00	
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NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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46,274
REGISTRATION NUMBER

AUTOMATIC BRIGHTNESS LIMITATION FOR AVOIDING VIDEO SIGNAL CLIPPING

Field of the Invention

This invention relates to a method and apparatus for avoiding signal clipping in a video signal by automatically controlling brightness limitations.

Background Art

Television circuits are commonly designed or modified so as to further integrate the functions thereof to enable operate with low power consumption. However, discrepancies can arise when the power supply is reduced. For example, a clipping effect may occur when the signals reach a minimum or maximum voltage level. The signal may deteriorate in shape in these circumstances.

As far as waveform is concerned, the television circuit required to maintain a signal with desired dynamic amplitude, even if the power supply is reduced. Therefore, preventive measures may be required with the implementation of a brightness limitation block to avoid the black reference voltage level and the video signals from reaching undesirable levels. Furthermore, the black reference voltage level should be controlled in a constant manner.

Summary of the Invention

In accordance with the present invention, there is provided a video signal processing system comprising, for each colour channel, a control circuit and clamping circuit for generating a colour channel reference signal and controlling a colour channel video signal, and a brightness limitation circuit coupled to receive the colour channel reference signal from each of the colour channels and coupled to provide a feedback signal to regulate a brightness level of each video signal according to a comparison of a minimum signal level amongst the colour channel reference signals and a fixed reference signal level.

Preferably the brightness limitation circuit comprises a minimum detection circuit for detecting and outputting a minimum signal level from amongst the colour channel reference signals, and a comparator having as inputs the fixed reference signal level and the minimum signal level, so as to produce the feedback signal as output. In a particular embodiment of the invention, the comparator is coupled to receive the minimum signal level at its negative input and the fixed reference signal level at its positive input.

Preferably each control circuit includes a plurality of adders coupled in the signal path of the corresponding colour channel reference signal, wherein the feedback signal is coupled as input to one of the adders. The feedback signal may be coupled from the brightness limitation circuit to the control circuit by way of a brightness control circuit which enables manual brightness adjustment of the colour channels.

In one form of the invention each control circuit includes an adder circuit coupled in the signal path of the corresponding colour channel video signal, wherein a feedback signal from the clamping circuit, generated according to the colour channel video signal and the colour channel reference signal, is coupled as input to the adder circuit.

The present invention also provides a video signal processing circuit for regulating colour channel video information signals, comprising a minimum signal detector for detecting a minimum signal level amongst a plurality of colour channel reference signals, a comparator which compares the minimum signal level with a fixed voltage reference signal and generates a corresponding output, and an additive feedback coupling of the comparator output signal and each of the colour channel reference signals.

The present invention further provides a video signal brightness controller, comprising:

a plurality of colour channel control means each coupled to receive as input a respective colour channel video signal and colour channel reference signal and generate a respective adjusted colour channel video signal and adjusted colour channel reference signal;

a plurality of clamping means, each clamping means corresponding to a respective colour channel control means and being coupled to receive as input the respective adjusted colour channel video signal and adjusted colour channel reference signal and produce a corresponding clamping feedback signal; and

a brightness limitation means coupled to receive the adjusted colour channel reference signal from each colour channel control means and produce a corresponding brightness feedback signal;

wherein each of the colour channel control means includes a first adder in path of the colour channel video signal, to which the clamping feedback signal is coupled, and a second adder in the path of the colour channel reference signal, to which the brightness feedback signal is coupled.

Brief Description of the Drawings

The invention is described in greater detail hereinafter, by way of example only, with reference to a preferred embodiment thereof and the accompanying drawings, wherein:

Figure 1 is a functional block diagram illustrating a known television signal control system;

Figure 2 is an illustration of a brightness curve;

Figures 3 and 4 illustrate of video signals from a known system;

Figure 5 is a circuit diagram of an output portion of a control block;

Figure 6 is a functional block diagram of a television signal control system incorporating a brightness limitation block according to an embodiment of the present invention;

Figure 7 is a block diagram of a brightness limitation circuit;

Figure 8 is a simplified functional block diagram of a video signal control system according to an embodiment of the present invention; and

Figure 9 shows several voltage range diagrams illustrating the operation of an embodiment of the invention.

Detailed Description of the Preferred Embodiments

Figure 1 shows a fundamental functional block diagram of an existing system 2 for controlling the signals of red, green and blue channels before these signals are distributed to the display tube of a television. Basically, this system includes, for each of the red, green and blue channels, a control block (4^R,4^G, 4^B)and a clamp block (6^R, 6^G, 6^B) , a brightness block 8, a cut-off (CO) fine tuning (DC) block 10 and a cut-off (CO) block 12. Since the control and clamp blocks are identical for each channel, only the red channel is discussed hereinbelow in the interests of clarity.

The control block 4 is mainly constructed using adders to control the video signals to present perfect pictures for display on the television screen. The appropriate CO brightness DC and clamping input signals are mixed together to generate accurate output signals, Rsignal, Gsignal, Bsignal, Rblack, Gblack and Bblack. The generated output Rsignal is an output signal that contains video information, while Rblack is an output signal that provides a black reference voltage level. The control block, however, is sensitive to the signals with low voltage, as discussed in greater detail hereinbelow.

The clamp block 6 receives Rsignal and Rblack as input signals from the control block 4. The clamp block is used to clamp the Rsignal signal, which means that Rsignal is aligned with the Rblack signal, as illustrated in Figure 2, to maintain a stable black level or picture brightness. The output signal from the clamp block 6, iclpR is fed back to the control block 4 to determine the amplitude difference between the Rsignal and Rblack signals for performing further alignment if necessary.

The brightness block 8 is used to adjust the black reference voltage level Rblack. Brightness can be adjusted by the user with the use of remote control or from the television set itself. The CO fine tuning (DC) block 10 is used to fine tune the black reference voltage level which is controlled by the internal circuit as described below. The signals for brightness adjustment consists of ibriR, ibriG and ibriB, and the signals for DC adjustment comprise idcR, idcG and idcB, and are passed to the respective control blocks (Figure 1).

The cut off block 12 is used to control the red, green and blue electron guns so as to provide an accurate black reference voltage level. This is required because signals for the electron guns have a high spread. Manual cut off adjustment is usually performed at the manufacturing stage. Tuning has to be done if the quality of one colour is different from a defined colour. This adjustment is made with the use of a potentiometer or by bus control whereby information is stored in a memory circuit of the television. On the other hand, automatic cut off adjustment can be done with a feedback loop configuration. Both methods allow correction signals of icoR, icoG and icoB to be varied from Vco(min) to Vco(max) as shown in Figure 2.

With reference to Figure 2, Rblack is an output signal that provides a black reference voltage level which is used for clamping purpose so that a constant black level can be maintained. Rsignal is an output signal which contains the red channel video information. A maximum signal clipping zone and minimum signal clipping zone are indicated in the figure and are referred to as forbidden zones, whereby both Rsignal and Rblack signals are prohibited from falling into these zones. However, the Rsignal signal can be fine tuned and adjusted with three adjustments. Namely, cut-off (CO) adjustment, brightness adjustment and CO fine tuning (DC) adjustment. Taking Vrblck as the black reference voltage level, the Rblack signal is able to swing from Vco(min) to Vco(max) when CO adjustment is being tuned. Similarly the Rblack signal is able to swing from Vbri(min) to Vbri(max) when brightness adjustment is being tuned. Likewise, the Rblack signal is able swing from Vdc(min) to Vdc(max) when DC adjustment is being tuned. During initialization, at time tl, when the television set is turned on, the Rsignal signal has to be aligned along the Rblack signal progressively. Alternately, alignment has to be made when any of the three adjustments has been fine tuned or adjusted. As a result, the signal of Rsignal also has a constant black level as it is in line with the Rblack signal.

Total adjustment is the addition of CO adjustment, brightness adjustment and DC adjustment. An equation of for the overall adjustment Vtotal is as shown below:

Total adjustment = CO adjustment + brightness adjustment + DC adjustment (Equ. 1)

$$Vtotal = Vco + Vbri + Vdc \quad \text{(Equ. 2)}$$

Figure 3 illustrates a video signal obtained from an existing system that operates with a 9 Volt power supply. Various voltages for the system as shown in Table 1, below, are based on assumption only.

Table 1

Names of Waveform	Voltage (Volt)
Black to White (B/W) Pulse	3 Vp-p
Vrblck (typical)	3 volts
Vco (Maximum/Minimum)	+/- 1 Volt
Vbri (Maximum/Minimum)	+/- 0.9 Volt
Vdc (Maximum/Minimum)	+/- 0.15 Volt

To compute the voltages of Vtotal(max) and Vtotal(min)

Vtotal = Vco + Vbri + Vdc from (Equ. 2)

Vtotal(max) = (1 + 0.9 + 0.15) Volts

= +2.05 Volts

Vtotal = Vco + Vbri + Vdc from (Equ. 2)

Vtotal(min) = (-1 -0.9 -0.15)Volts

= -2.05 Volts

Typically, Rblack signal is set at the black reference voltage level (Vrblck) which is 3 Volts. Based on the calculation as shown above, this signal is allowed to swing positive by 2.05 Volts and negative by 2.05 Volts. In other words, it is able to vary from 0.95 Volt to 5.05 Volts. A further 3 Volts is required by the black to white (B/W) pulse with the contrast level set to maximum. Hence, the maximum level of the video signal is 8.05 Volts. A voltage margin of 0.95 Volts is reserved for sharpness adjustment and over modulation to occur. As such neither of the Rsignal and Rblack signals falls into the maximum and minimum signal limitation zones.

Thus, no problem is encountered with typical video amplitude.

Figure 4 illustrates a video signal obtained from an existing system that operates with an 8 Volt power supply. The objective of power supply reduction is to achieve a system that is able to function with low power consumption. At the same time, it must be able to maintain a video signal with reasonable dynamic amplitude. However, difficulties have been encountered in these circumstances.

The black reference voltage level (Vrblck) is compensated to 2.2 Volts as the power supply is reduced by 1 Volt. Similarly, Vrblck is allowed to swing positive by 2.05 Volts and negative by 2.05 Volts. Likewise, 3 Volts is required by the black to white pulse with the contrast level set to maximum. Hence, the maximum level of the video signal is 7.25 Volts.

To compute the range of Vrblck level, consider the following:

Let Vrblck be the final result of the black reference voltage level, and
Vrblck(current) be the present black reference voltage level.

$$Vrblck = Vrblck(current) + Vtotal \qquad \text{(Equ. 3)}$$

Therefore, $Vrblck(maximum) = (2.2 + 2.05)$ Volts

$= \underline{4.25 \text{ Volts}}$

and $Vrblck(minimum) = (2.2 - 2.05)$ Volt

$= \underline{0.15 \text{ Volt}}$

Based on the calculated results, the Rblack signal is only allowed to vary from 0.15 Volts to 4.25 Volts in this instance. A voltage margin of 0.75 Volt is reserved for further B/W pulse adjustment as mentioned before. This implies that the maximum signal clipping zone is not affected, however the minimum signal clipping zone is affected by the Rblack signal.

Figure 5 shows a circuit 20 of an output portion of a control block. Basically, it consists of an emitter follower Q1 coupled to a transistor Q2 which is biased at a fixed voltage, Vbias. Assume that, the Rblack signal (OUT) is allowed to fall to a voltage level of Vrblck(minimum) which is

as low as 0.5 Volt. Based on the calculation as shown above, it shows that Rblack signal (OUT) has reached to a voltage level of 0.15 Volt. This implies that the Rblack signal has already fallen into the minimum signal limitation zone. Hence, the voltage level (Vrblck) of Rblack signal is too low for Q2 to function properly. As such, it causes Q2 to operate in saturation.

In order to alleviate this problem, the television circuit can be equipped with a brightness limitation block, which can provide the following:

1. Prevention of the black reference voltage level (Rblack) and the video signal (Rsignal) from entering into the minimum signal clipping zone.
2. Provision of the brightness block with a precise correction signal, limiting the brightness.
3. Maintenance of a constant black reference voltage level at Vrblck minimum.
4. Maintenance of a video signal with dynamic amplitude.

In order to overcome the above mentioned difficulties, a brightness limitation block 32 can be implemented in the system 30 as shown in Figure 6. Signals of Rblack, Gblack, and Bblack from the respective control blocks 4^R, 4^G, 4^B are connected to the inputs of the brightness limitation block 32. The output of the brightness limitation block, Brilim is fed back to the brightness block 8. With this configuration, it contributes the difference between the existing system and the proposed system.

With reference to Figure 7, a simple exemplary implementation of the brightness limitation block 32 is shown, including a comparator 34. A minimum detector 36 is introduced before the input of the comparator, which can be easily done using diodes. The output of the minimum detector is applied to the negative input of the comparator while the positive input of the comparator is maintained with a fixed voltage, Vrblck (minimum) with respect to ground.

The function of the minimum detector 36 is to select only one of the three input signals with the lowest voltage. Subsequently, this signal is reflected on the output of the minimum detector.

A comparison is made between the voltage at the negative input and the positive input of the comparator 34. If the voltage at the negative input is less than Vrblck(minimum) at the positive

input of the comparator, a signal will be generated at the output, Brilim. The signal at Brilim will correspond to the amplitude between Vrblck(minimum) and the signal at the negative input of the comparator. This correction signal is fedback to the input of the brightness block 8. As such, the signal of Rblack is prohibited from entering the minimum signal clipping zone.

On the other hand, if the voltage at the negative input is greater than the Vrblck(minimum) at the positive input of the comparator, no signal is generated at the output, Brilim. Therefore, it is not necessary to add to the signal being passed to the brightness block as it did not enter beyond the minimum signal clipping zone.

Figure 8 shows a simplified block diagram of the circuit 30 shown in Figure 6 (for the red channel only), to further elaborate the detailed operation of the new system. Basically, the control block 4 comprises four adders: three adders are included along the Rblack signal path and one adder is included along the Rsignal path. The brightness block 8 is used to provide brightness adjustment, the CO fine tuning block 10 is used to provide DC adjustment, and the Cut-Off block 12 is used to provide CO adjustment.

As described above, if the Rblack signal from the control block 4 is less than Vrblck(minimum), a correction signal, Brilim, will be generated and fedback to the brightness block. In the brightness block the correction signal, Brilim, may be combined with a manual brightness adjustment signal, using an adder or the like, to form the ibriR signal provided to the control block. Subsequently, this signal is added to the Rblack signal so as to avoid it from falling into the minimum signal limitation zone.

Alignment is performed with the use of the clamp block 6. A comparison is made between the Rblack and Rsignal signals. An iclpR signal is then generated at the output of the clamp block which indicates the amplitude difference of both signals if they are different. Eventually, iclpR signal is added into the Rsignal signal. As such, the Rsignal signal is superimposed on the Rblack signal and alignment has been done.

Example calculations are set forth below to illustrate how the Rblack signal is prevented from

entering the minimum signal limitation zone with the implementation of the brightness limitation block as described above.

Example 1

Assume that Vrblck(current) = 2.2 volts,

Vco(minimum) = -1 Volt,

Vdc(minimum) = -0.15 Volt,

and the brightness limitation block is intended to prevent Vrblck from falling below 0.5 Volt. It is possible then to determine what is the Vbri(minimum) that is required to be added into the control block.

Vrblck = Vrblck(current) - Vco - Vdc - Vbri from (Equ. 3)

0.5 = 2.2 - 1 - 0.15 - Vbri

Thus, Vbri = -0.55 Volt , ideally Vbri(minimum) = -0.9 Volt

Therefore, Vbri from the brightness block would be greater than -0.55 Volt, otherwise, it will cause Vrblck to fall into the minimum signal limitation zone. This indicates that there is a significant increase of voltage, Vbri from -0.9 Volt to -0.55 volt, to provide the correction (refer Figure 9).

Example 2

Assume that Vrblck(current) = 2.2 Volts,

Vco = -0.8 Volt, and

Vdc (minimum) = -0.15 Volt.

It is possible then to determine the minimum Vbri.

Vrblck = Vrblck(current) - Vco - Vdc - Vbri from (Equ. 3)

0.5 = 2.2 - 0.8 0.15 - Vbri

Hence, Vbri = -0.75 Volt , ideally minimum Vbri = -0.9 Volt

Therefore, Vbri from the brightness block should not be greater than -0.75 Volt. This indicates that there is a significant increase of voltage Vbri, from -0.9 Volt to -0.75 Volt, to provide the correction (Refer figure 9).

Based on simulation results of this system, it has been shown that the black reference voltage level and the video signal are prevented from entering into the minimum signal clipping zone. Moreover, a constant black reference voltage level and the video signal with dynamic amplitude are maintained.

The foregoing detailed description of the preferred implementations of the present invention has been presented by way of example only, and is not intended to be considered limiting to the invention as defined in the appended claims.

Throughout this specification and the claims which follow, unless the context requires otherwise, the word "comprise", and variations such as "comprises" and "comprising", will be understood to imply the inclusion of a stated integer or step or group of integers or steps but not the exclusion of any other integer or step or group of integers or steps.

Claims

1. A video signal processing system comprising, for each colour channel, a control circuit and clamping circuit for generating a colour channel reference signal and controlling a colour channel video signal, and a brightness limitation circuit coupled to receive the colour channel reference signal from each of the colour channels and coupled to provide a feedback signal to regulate a brightness level of each video signal according to a comparison of a minimum signal level amongst the colour channel reference signals and a fixed reference signal level.

2. A video signal processing system as claimed in claim 1, wherein the brightness limitation circuit comprises a minimum detection circuit for detecting and outputting a minimum signal level from amongst the colour channel reference signals, and a comparator having as inputs said fixed reference signal level and said minimum signal level, and producing said feedback signal as output.

3. A video signal processing system as claimed in claim 2, wherein said comparator is coupled to receive said minimum signal level at its negative input and said fixed reference signal level at its positive input.

4. A video signal processing system as claimed in claim 2 or 3, wherein each said control circuit includes a plurality of adders coupled in the signal path of the corresponding colour channel reference signal, and wherein said feedback signal is coupled as input to one of said adders.

5. A video signal processing system as claimed in claim 4, wherein said feedback signal is coupled from the brightness limitation circuit to the control circuit by way of a brightness control circuit which enables manual brightness adjustment of the colour channels.

6. A video signal processing system as claimed in claim 5, wherein said brightness control circuit incorporates an adder for combining the feedback signal with a manual brightness adjustment signal.

7. A video signal processing system as claimed in claim 4, further including at least one cut-off adjustment circuit coupled to provide input to a respective adder in the signal path of the colour channel reference signal in each control circuit.

8. A video signal processing system as claimed in any one of claims 1 to 7, wherein each said control circuit includes an adder circuit coupled in the signal path of the corresponding colour channel video signal, and wherein a feedback signal from said clamping circuit, generated according to the colour channel video signal and the colour channel reference signal, is coupled as input to the adder circuit.

9. A video signal processing circuit for regulating colour channel video information signals, comprising a minimum signal detector for detecting a minimum signal level amongst a plurality of colour channel reference signals, a comparator which compares said minimum signal level with a fixed voltage reference signal and generates a corresponding output, and an additive feedback coupling of said comparator output signal and each of said colour channel reference signals.

10. A video signal processing circuit as claimed in claim 9, including a brightness control circuit for adjusting the video signal brightness level by manual adjustment of said colour channel reference signals, wherein said additive feedback coupling of said comparator output signal is coupled through said brightness control circuit.

11. A video signal brightness controller, comprising:

a plurality of colour channel control means each coupled to receive as input a respective colour channel video signal and colour channel reference signal and generate a respective adjusted colour channel video signal and adjusted colour channel reference signal;

AMENDED CLAIMS
[received by the International Bureau on 03 March 1999 (03.03.99); new claim 13 added; remaining claims unchanged (1 page)]

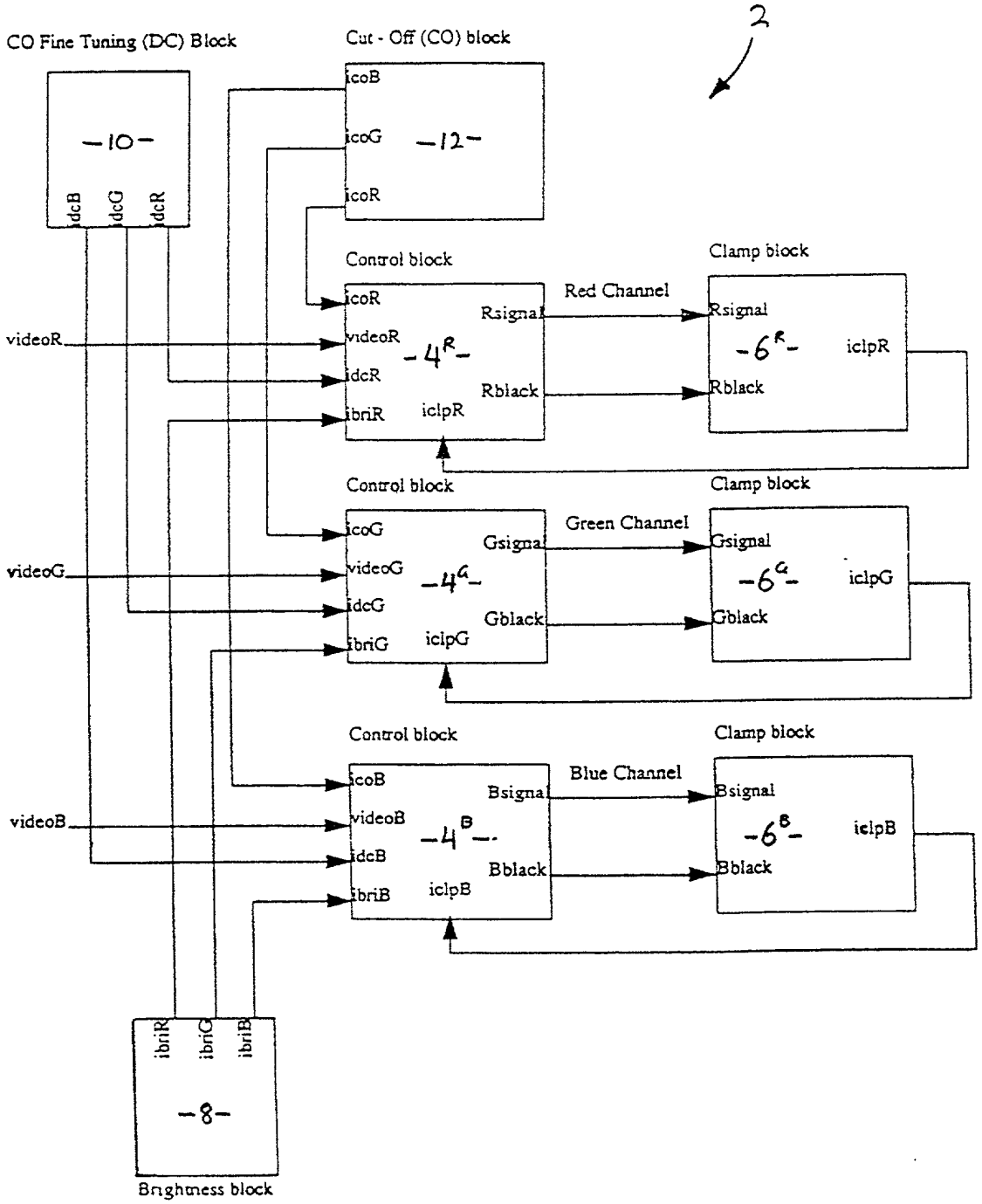
a plurality of clamping means, each clamping means corresponding to a respective colour channel control means and being coupled to receive as input the respective adjusted colour channel video signal and adjusted colour channel reference signal and produce a corresponding clamping feedback signal; and

a brightness limitation means coupled to receive the adjusted colour channel reference signal from each colour channel control means and produce a corresponding brightness feedback signal;

wherein each said colour channel control means includes a first adder in path of the colour channel video signal, to which said clamping feedback signal is coupled, and a second adder in the path of the colour channel reference signal, to which said brightness feedback signal is coupled.

12. A video signal brightness controller as claimed in claim 11, wherein said brightness limitation means comprises a minimum signal level detector for detecting a minimum signal level amongst the plurality of adjusted colour channel reference signals, and a comparator for generating said brightness feedback signal on the basis of the detected minimum signal level and a fixed reference signal level.

13. A method for regulating colour channel video information signals, comprising the steps of detecting a minimum signal level amongst a plurality of colour channel reference signals, comparing said minimum signal level with a fixed voltage reference signal and generating a corresponding comparator output, and providing an additive feedback coupling of said comparator output signal and each of said colour channel reference signals.


2
CO Fine Tuning (DC) Block
Cut - Off (CO) block
-10-
idcB
idcG
idcR
icoB
icoG
-12-
icoR
Control block
Clamp block
Red Channel
icoR
videoR
-4R-
idcR
ibriR
iclpR
Rsignal
Rblack
Rsignal
-6R-
iclpR
Rblack
videoR
Control block
Clamp block
Green Channel
icoG
videoG
-4G-
idcG
ibriG
iclpG
Gsignal
Gblack
Gsignal
-6G-
iclpG
Gblack
videoG
Control block
Clamp block
Blue Channel
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videoB
-4B-
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videoB
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Brightness block

Figure 1

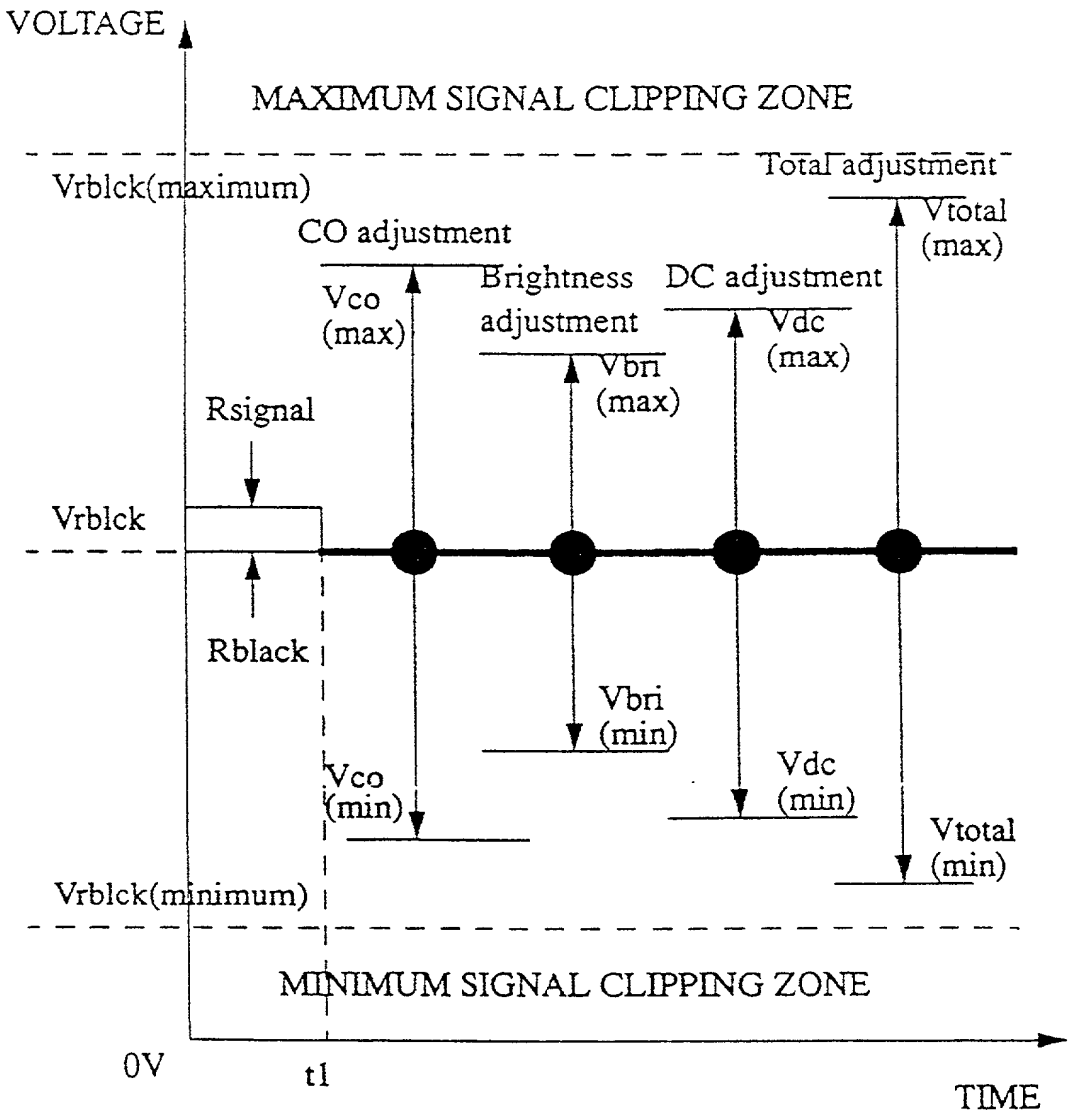
VOLTAGE
MAXIMUM SIGNAL CLIPPING ZONE
Total adjustment
Vrblck(maximum)
Vtotal (max)
CO adjustment
Vco (max)
Brightness adjustment
DC adjustment
Vdc (max)
Vbri (max)
Rsignal
Vrblck
Rblack
Vbri (min)
Vdc (min)
Vco (min)
Vtotal (min)
Vrblck(minimum)
MINIMUM SIGNAL CLIPPING ZONE
0V
t1
TIME

Figure 2

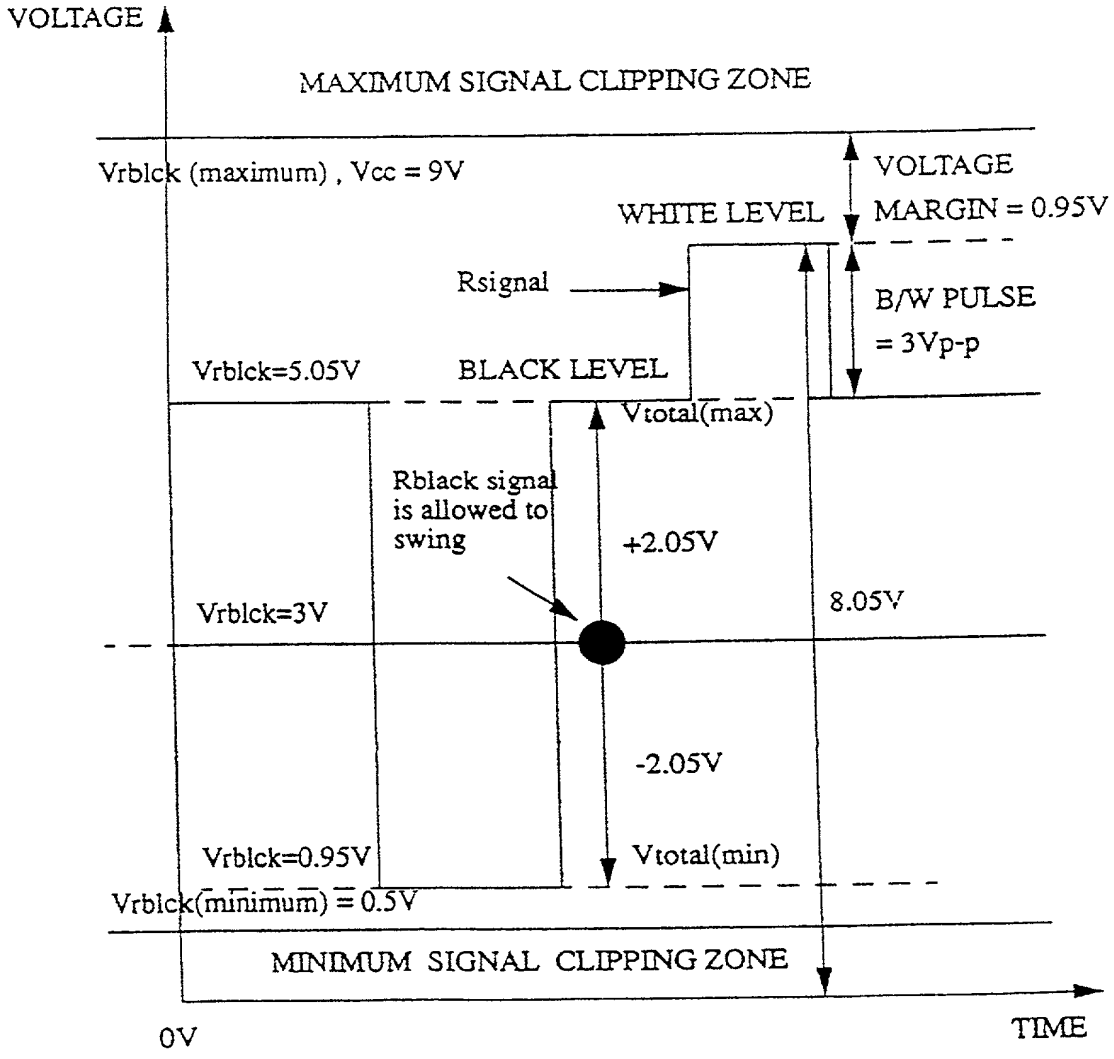
VOLTAGE
MAXIMUM SIGNAL CLIPPING ZONE
Vrblck (maximum) , Vcc = 9V
VOLTAGE
MARGIN = 0.95V
WHITE LEVEL
Rsignal
B/W PULSE
= 3Vp-p
Vrblck=5.05V
BLACK LEVEL
Vtotal(max)
Rblack signal
is allowed to
swing
+2.05V
8.05V
Vrblck=3V
-2.05V
Vrblck=0.95V
Vtotal(min)
Vrblck(minimum) = 0.5V
MINIMUM SIGNAL CLIPPING ZONE
0V
TIME

Figure 3

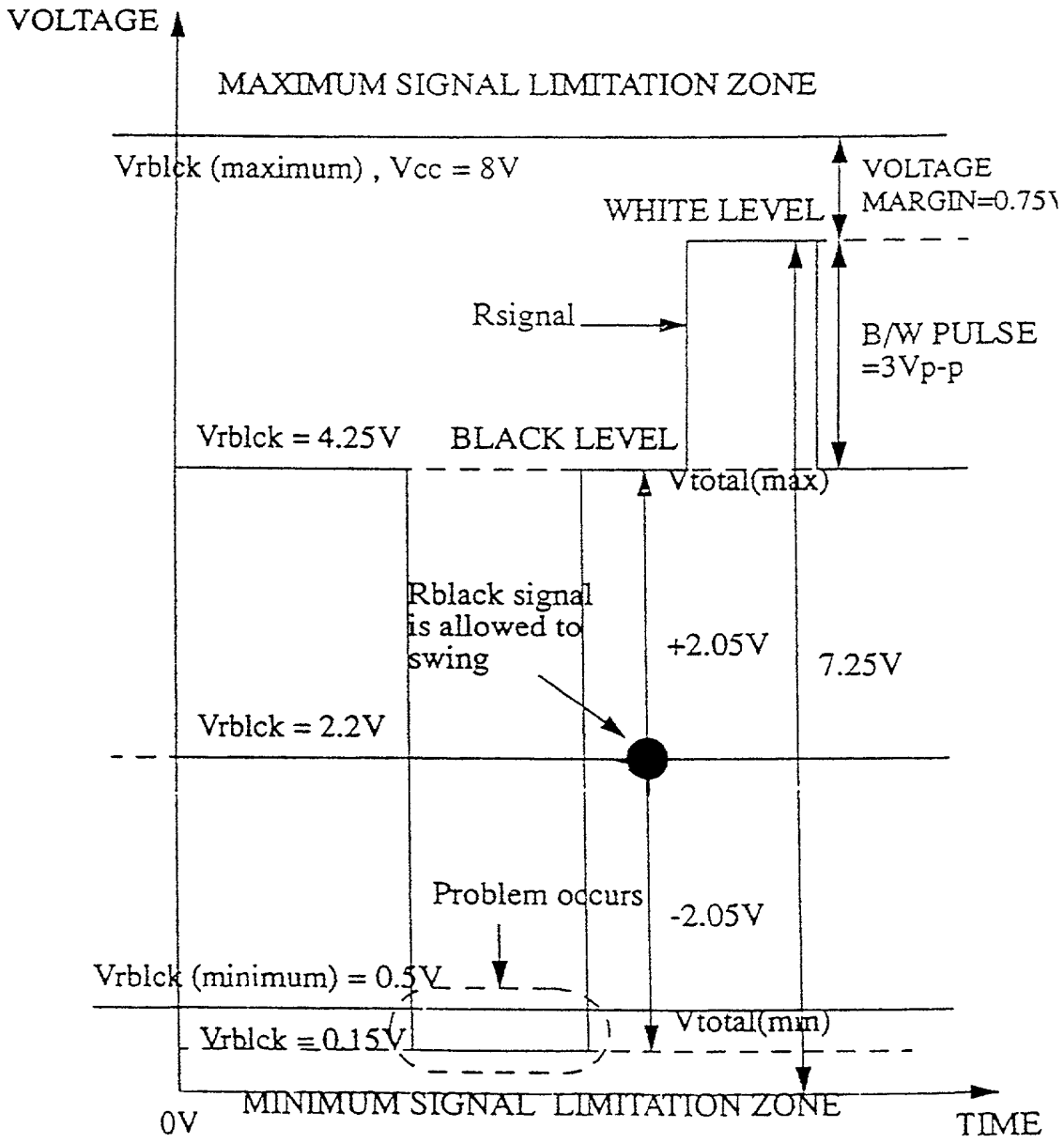
VOLTAGE
MAXIMUM SIGNAL LIMITATION ZONE
Vrblck (maximum) , Vcc = 8V
VOLTAGE MARGIN=0.75V
WHITE LEVEL
Rsignal
B/W PULSE =3Vp-p
Vrblck = 4.25V
BLACK LEVEL
Vtotal(max)
Rblack signal is allowed to swing
+2.05V
7.25V
Vrblck = 2.2V
Problem occurs
-2.05V
Vrblck (minimum) = 0.5V
Vrblck = 0.15V
Vtotal(min)
MINIMUM SIGNAL LIMITATION ZONE
0V
TIME

Figure 4

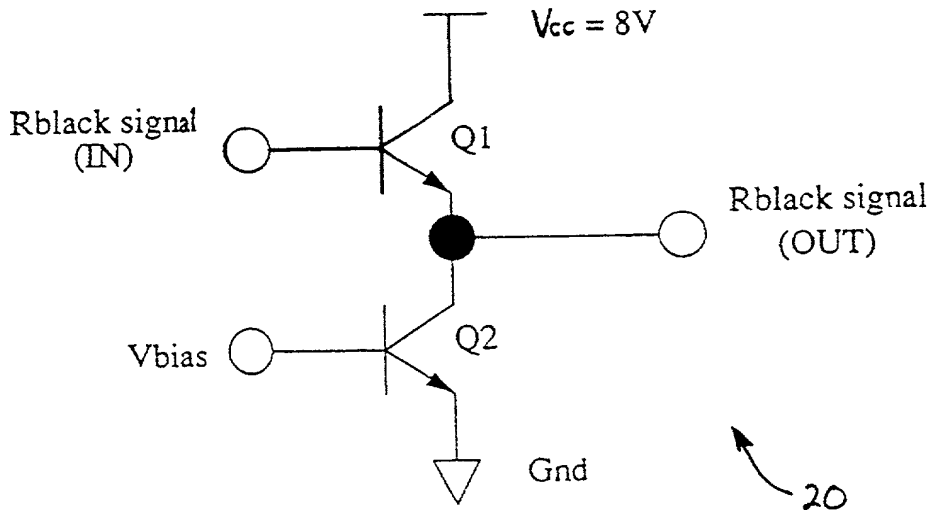

Figure 5

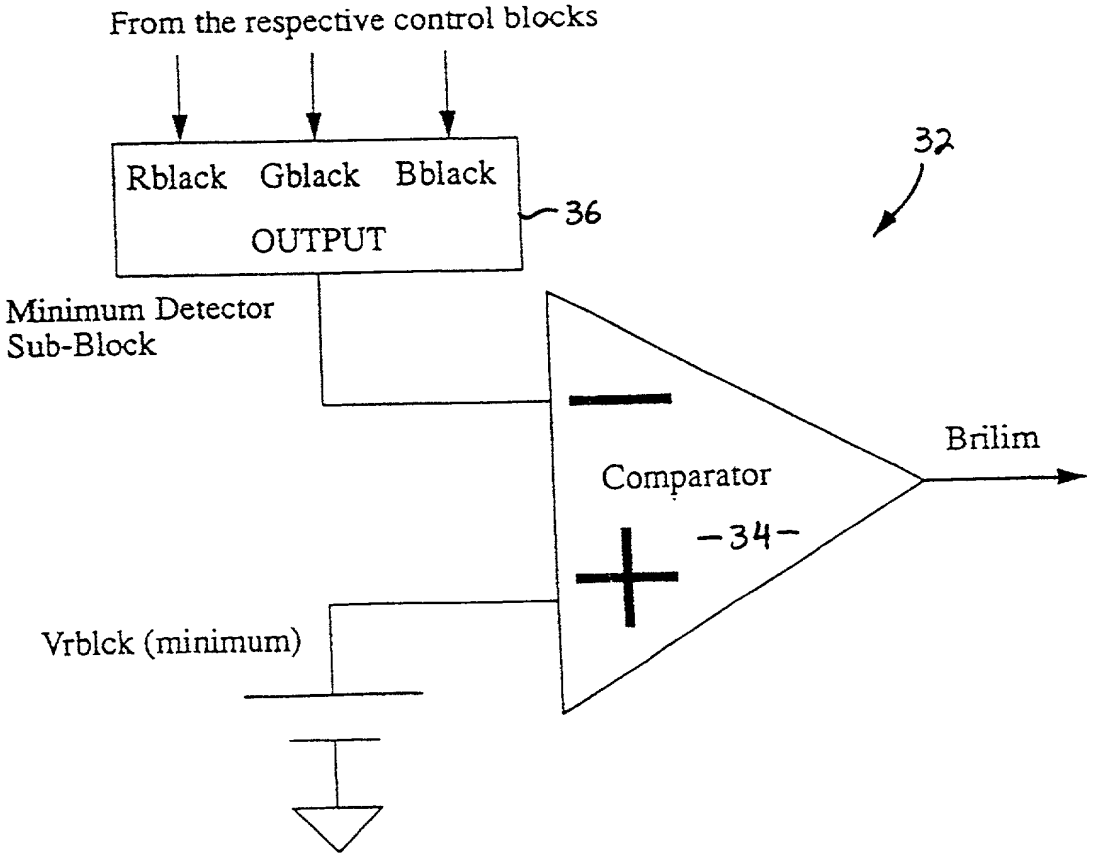

Figure 7

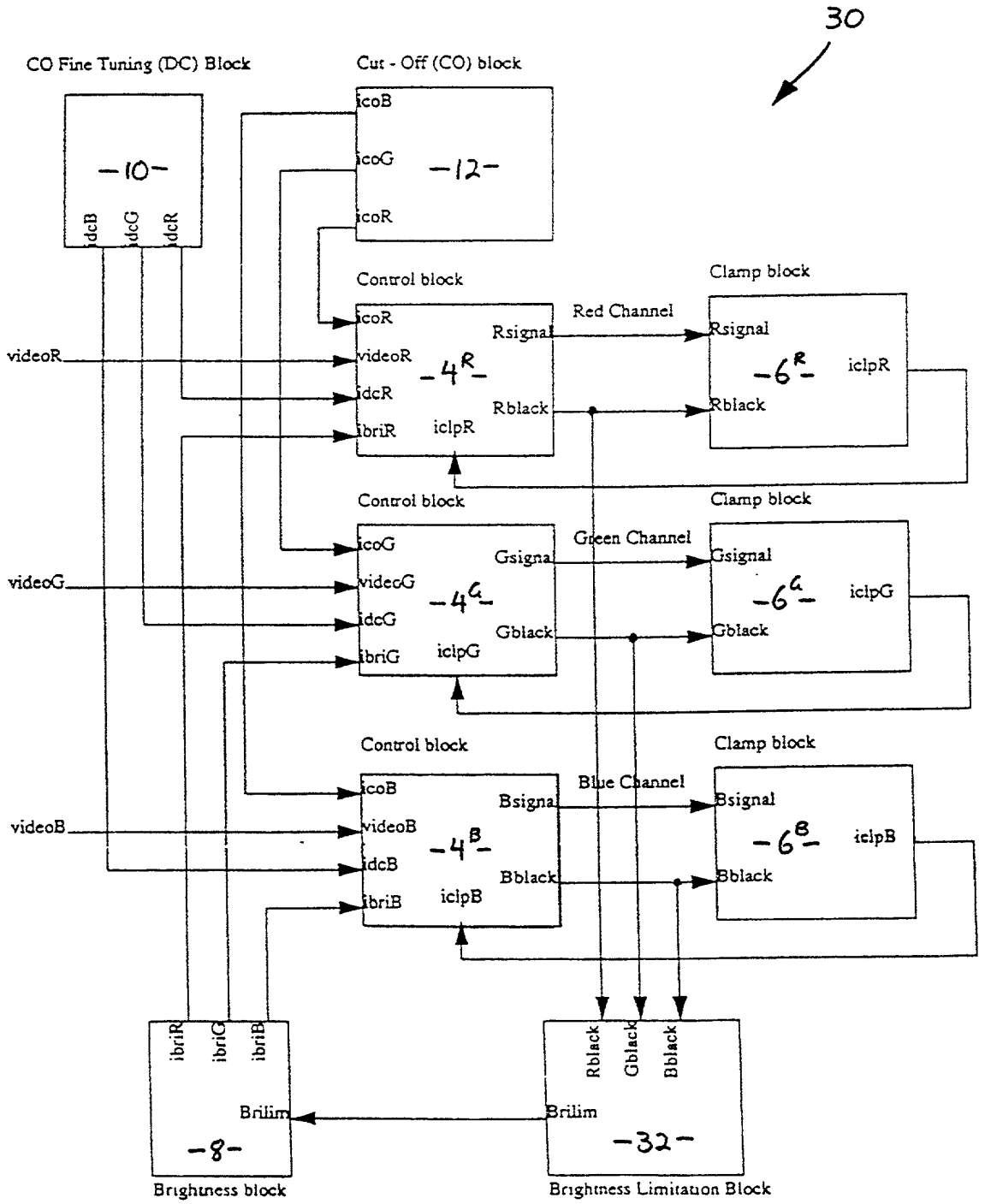
30
CO Fine Tuning (DC) Block
Cut - Off (CO) block
-10-
idcB
idcG
idcR
icoB
icoG
-12-
icoR
Control block
Clamp block
Red Channel
icoR
videoR
idcR
ibriR
-4R-
Rsignal
Rblack
iclpR
Rsignal
-6R-
Rblack
iclpR
videoR
Control block
Clamp block
Green Channel
icoG
videoG
idcG
ibriG
-4G-
Gsigna
Gblack
iclpG
Gsignal
-6G-
Gblack
iclpG
videoG
Control block
Clamp block
Blue Channel
icoB
videoB
idcB
ibriB
-4B-
Bsigna
Bblack
iclpB
Bsignal
-6B-
Bblack
iclpB
videoB
ibriR
ibriG
ibriB
Brilim
-8-
Brightness block
Rblack
Gblack
Bblack
Brilim
-32-
Brightness Limitation Block

Figure 6

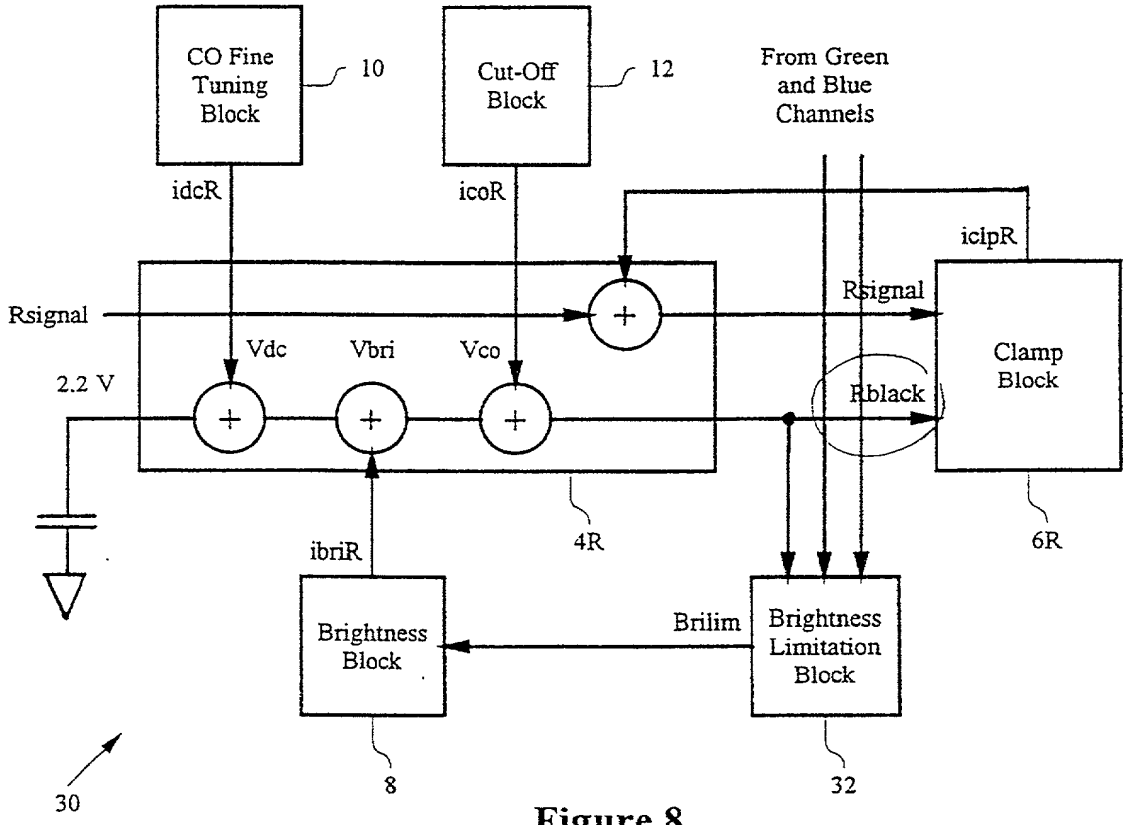
CO Fine Tuning Block
10
Cut-Off Block
12
From Green and Blue Channels
idcR
icoR
iclpR
Rsignal
Rsignal
Vdc
Vbri
Vco
2.2 V
Rblack
Clamp Block
4R
6R
ibriR
Brightness Block
Brilim
Brightness Limitation Block
8
32
30

Figure 8

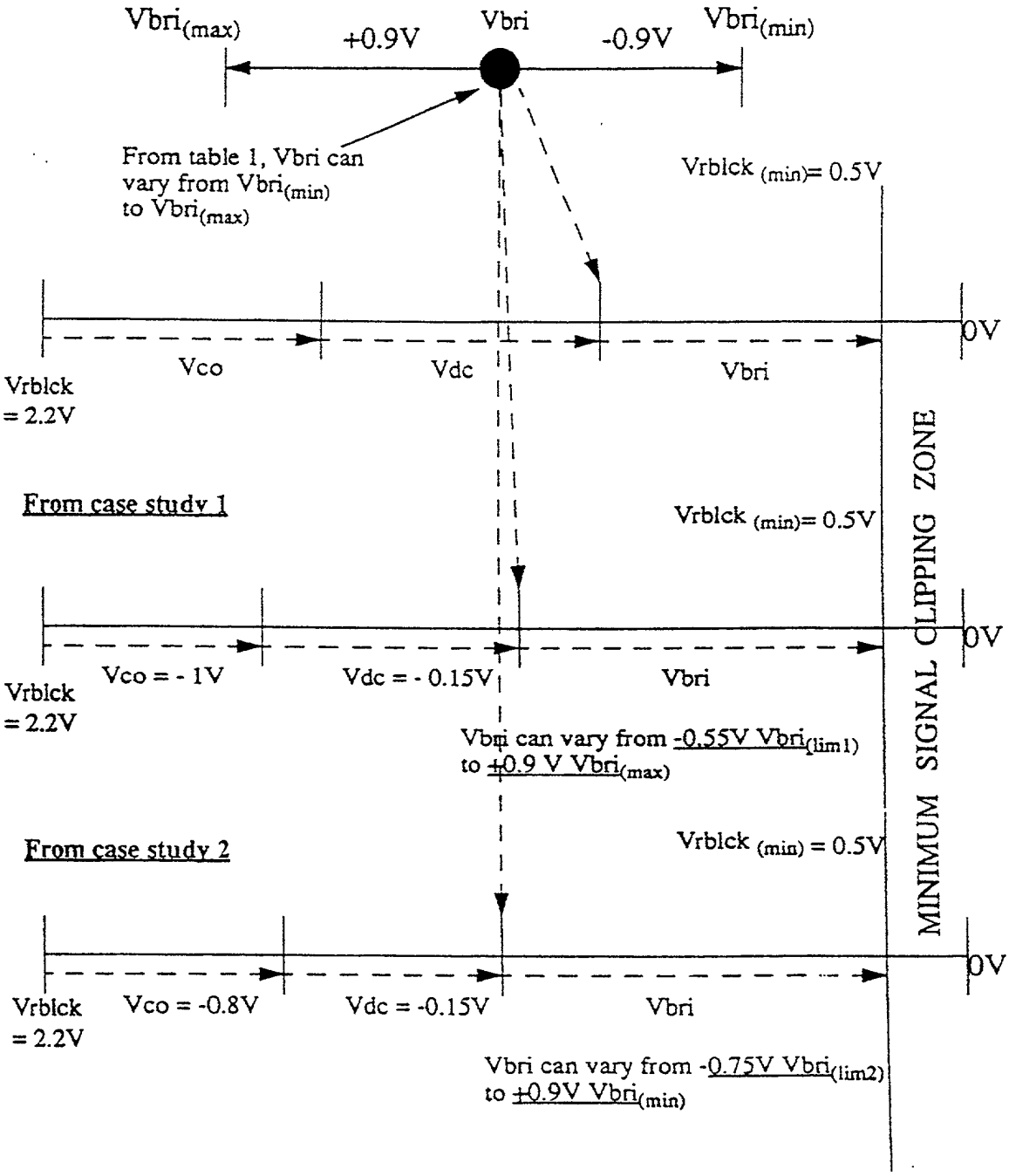
Vbri(max)
+0.9V
Vbri
-0.9V
Vbri(min)
From table 1, Vbri can vary from Vbri(min) to Vbri(max)
Vrblck (min)= 0.5V
0V
Vco
Vdc
Vbri
Vrblck = 2.2V
From case study 1
Vrblck (min)= 0.5V
0V
Vco = - 1V
Vdc = - 0.15V
Vbri
Vrblck = 2.2V
Vbri can vary from -0.55V Vbri(lim1) to +0.9 V Vbri(max)
MINIMUM SIGNAL CLIPPING ZONE
From case study 2
Vrblck (min) = 0.5V
0V
Vrblck = 2.2V
Vco = -0.8V
Vdc = -0.15V
Vbri
Vbri can vary from -0.75V Vbri(lim2) to +0.9V Vbri(min)

Figure 9

99H00071 US

Docket No._____

DECLARATION AND POWER OF ATTORNEY UNDER 35 USC § 371(c)(4)FOR PCT APPLICATION FOR UNITED STATES PATENT (1/3)

As a below named inventor, I hereby declare that:
my residence, post office address and citizenship are as stated below under my name;

I verily believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought, namely the invention entitled
WIRE ROD ROLLING LINE
described and claimed in international application number PCT/JP00/00814 filed on February 15, 2000
I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.
I acknowledge the duty to disclose to the Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56.
Under Title 35, U.S. Code § 119, the priority benefits of the following foreign application(s) filed within one year prior to my international application are hereby claimed:
Japanese Patent Application No. 11-037812 filed on February 16, 1999
Japanese Patent Application No. 11-055925 filed on March 3, 1999
Japanese Patent Application No. 11-227623 filed on August 11, 1999
The following application(s) for patent or inventor's certificate on this invention were filed in countries foreign to the United States of America either (a) more than one year prior to my international application, or (b) before the filing date of the above-named foreign priority application(s):

I hereby appoint the following as my attorneys of record with full power of substitution and revocation to prosecute this application and to transact all business in the Patent Office:

James A. Oliff, Reg. No.27,075; William P. Berridge, Reg. No.30,024;
Kirk M. Hudson, Reg. No.27,562; Thomas J. Pardini, Reg. No.30,411;
Edward P. Walker, Reg. No.31,450; Robert A. Miller, Registration No.32,771; and
Mario A. Costantino, Registration No.33,565.

ALL CORRESPONDENCE IN CONNECTION WITH THIS APPLICATION SHOULD BE SENT TO OLIFF & BERRIDGE, P.O.BOX 19928, ALEXANDRIA, VIRGINIA 22320, TELEPHONE(703)836-6400.

I hereby declare that I have reviewed and understand the contents of this Declaration, and that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

1 *Typewritten Full Name of Sole or First Inventor*: Ryo (Given Name) | Middle Initial | Takeda (Family Name)

2 Inventor's Signature: Ryo Takeda

3 Date of Signature: September (Month) 29 (Day) 2000 (Year)

Residence: Kurashiki (City) JPX Okayama (State or Province) JAPAN (Country)

Citizenship: Japanese

Post Office Address (Insert complete mailing address, including country): c/o Technical Research Laboratories, Kawasaki Steel Corporation, Kawasakidori 1-chome, Mizushima, Kurashiki-shi, Okayama 712-8074 JAPAN

Note to Inventor: Please sign name on line 2 exactly as it appears in line 1 and insert the actual date of signing on line 3.

IF THERE IS MORE THAN ONE INVENTOR USE PAGE 2 AND PLACE AN "X"HERE ☒

99F00041

(Discard this page in a sole inventor application) (2/3)

1 *Typewritten Full Name of Joint Inventor*: Takao (Given Name) — (Middle Initial) Ogawa (Family Name)

2 Inventor's Signature: Takao Ogawa

3 Date of Signature: September (Month) 29 (Day) 2000 (Year)

Residence: Kurashiki (City) Okayama (State or Province) JAPAN (Country)

Citizenship: Japanese

Post Office Address: (Insert complete mailing address, including country) c/o Technical Research Laboratories , Kawasaki Steel Corporation, Kawasakidori 1-chome, Mizushima, Kurashiki-shi, Okayama 712-8074 JAPAN

1 *Typewritten Full Name of Joint Inventor*: Given Name / Middle Initial / Family Name

2 Inventor's Signature

3 Date of Signature: Month / Day / Year

Residence: City / State or Province / Country

Citizenship:

Post Office Address: (Insert complete mailing address, including country)

1 *Typewritten Full Name of Joint Inventor*: Given Name / Middle Initial / Family Name

2 Inventor's Signature

3 Date of Signature: Month / Day / Year

Residence: City / State or Province / Country

Citizenship:

Post Office Address: (Insert complete mailing address, including country)

1 *Typewritten Full Name of Joint Inventor*: Given Name / Middle Initial / Family Name

2 Inventor's Signature

3 Date of Signature: Month / Day / Year

Residence: City / State or Province / Country

Citizenship:

Post Office Address: (Insert complete mailing address, including country)

Note to Inventor: Please sign name on line 2 exactly as it appears in line 1 and insert the actual date of signing on line 3.

This form may be executed only when attached to the first page of the Declaration and Power of Attorney of the application to which it pertains.

(Dis[redacted]d this page in a sole inventor a[redacted]cation) (3/3) 99Fm-21

1 *Typewritten Full Name of Joint Inventor* — Shigeharu (Given Name) — Middle Initial — Ochi (Family Name)

2 Inventor's Signature: Shigeharu Ochi

3 Date of Signature: September (Month) 29 (Day), 2000 (Year)

Residence: Niihama (City) JPX Ehime (State or Province) JAPAN (Country)

Citizenship: Japanese

Post Office Address: (Insert complete mailing address, including country) c/o Sumitomo Heavy Industries, Ltd., 5-2, Soubirakicho, Niihama-shi, Ehime 792-8588 Japan

1 *Typewritten Full Name of Joint Inventor* — Takeshi (Given Name) — Middle Initial — Tange (Family Name)

2 Inventor's Signature: TAKESHI TANGE

3 Date of Signature: September (Month) 29 (Day), 2000 (Year)

Residence: Niihama (City) JPX Ehime (State or Province) Japan (Country)

Citizenship: Japanese

Post Office Address: (Insert complete mailing address, including country) c/o Sumitomo Heavy Industries, Ltd., 5-2, Soubirakicho, Niihama-shi, Ehime 792-8588 Japan

1 *Typewritten Full Name of Joint Inventor* — Given Name — Middle Initial — Family Name

2 Inventor's Signature

3 Date of Signature — Month — Day — Year

Residence: City — State or Province — Country

Citizenship:

Post Office Address: (Insert complete mailing address, including country)

1 *Typewritten Full Name of Joint Inventor* — Given Name — Middle Initial — Family Name

2 Inventor's Signature

3 Date of Signature — Month — Day — Year

Residence: City — State or Province — Country

Citizenship:

Post Office Address: (Insert complete mailing address, including country)

Note to Inventor: Please sign name on line 2 exactly as it appears in line 1 and insert the actual date of signing on line 3.

This form may be executed only when attached to the first page of the Declaration and Power of Attorney of the application to which it pertains.